Amendments to the Claims

This listing will replace all prior versions and listings of claims in the application:

Listing of Claims

Claim 1. (currently amended) An electrical interconnect structure on a substrate, comprising:

a first low k or ultra low k dielectric layer;

a low k CMP protective layer disposed on said first low k dielectric layer; and

a CVD hardmask/CMP polish stop layer;

wherein said low k CMP protective layer is covalently bonded to said first low k dielectric layer.

Claim 2. (original) The electrical interconnect structure of claim 1, wherein said first low k dielectric layer is a first spin-on low k dielectric layer.

Claim 3. (original) The electrical interconnect structure of claim 1, wherein said first low k dielectric layer is comprised of an organic dielectric material.

Claim 4. (original) The electrical interconnect structure of claim 2, wherein said spin-on low k dielectric layer is selected from the group consisting of: SiLK™, GX-3™, porous SiLK™, GX-3p™, JSR LKD 5109™, porous spin-on $Si_wC_xO_yH_z$ material, spin-on dielectric material, low k spin-on dielectric material and porous low k spin-on dielectric material.

Claim 5. (original) The electrical interconnect structure of claim 1, wherein said low k CMP protective layer is a spin-on low k CMP protective layer.

Claim 6. (canceled)

Claim 7. (original) The electrical interconnect structure of claim 5, wherein said spin-on low k CMP protective layer is comprised of a material with a low CMP polish rate that can be directly polished without scratching or producing other defects.

Claim 8. (original) The electrical interconnect structure of claim 5, wherein said spin-on low k CMP protective layer has a dielectric constant of from about 2.2 to about 3.5.

Claim 9. (original) The electrical interconnect structure of claim 5, wherein said spin-on low k CMP protective layer is inert to chemicals contained in CMP polish slurries.

Claim 10. (currently amended) ~~The~~An electrical interconnect structure ~~of claim 5,~~ on a substrate, comprising:

a first low k or ultra low k dielectric layer;

a low k CMP protective layer disposed on said first low k dielectric layer; and

a CVD hardmask/CMP polish stop layer;

wherein said low k CMP protective layer is a spin-on low k CMP protective layer; and

wherein said spin-on low k CMP protective layer has molecular level free volume or molecular level porosity.

Claim 11. (original) The electrical interconnect structure of claim 10, wherein said molecular level free volume has a size ranging from about 2 Å to about 50 Å.

Claim 12. (original) The electrical interconnect structure of claim 10, wherein said molecular level porosity has a volume percent from about 5% to about 80%.

Claim 13. (currently amended) ~~The electrical interconnect structure of claim 5,~~ An electrical interconnect structure on a substrate, comprising:

a first low k or ultra low k dielectric layer;

a low k CMP protective layer disposed on said first low k dielectric layer; and

a CVD hardmask/CMP polish stop layer;

wherein said low k CMP protective layer is a spin-on low k CMP protective layer; and

wherein said spin-on low k CMP protective layer mechanically behaves like a sponge, which provides damping capability under application of down force during polish.

Claim 14. (currently amended) ~~The electrical interconnect structure of claim 5,~~ An electrical interconnect structure on a substrate, comprising:

a first low k or ultra low k dielectric layer;

a low k CMP protective layer disposed on said first low k dielectric layer; and

a CVD hardmask/CMP polish stop layer;

wherein said low k CMP protective layer is a spin-on low k CMP protective layer; and

wherein said spin-on low k CMP protective layer has fine and evenly dispersed pores.

Claim 15. (original) The electrical interconnect structure of claim 5, wherein said CMP protective layer is comprised of a spin-on material selected from the group consisting of: HOSP™, AP 6000™, HOSP BESt™, Ensemble™ Etch Stop, Ensemble™ Hard Mask, organo silsesquioxane, hydrido silsesquioxane, hydrido-organo silsesquioxane copolymer, siloxane, and silsesquioxane.

Claim 16. (original) The electrical interconnect structure of claim 15, wherein said spin-on material has a low dielectric constant and low CMP polish rate.

Claim 17. (original) The electrical interconnect structure of claim 1, wherein said CVD hardmask/CMP polish stop layer is a conventional CVD hardmask/CMP polish stop layer.

Claim 18. (original) The electrical interconnect structure of claim 17, wherein said hardmask / CMP polish stop layer is comprised of BLOk™, silicon nitride, silicon carbide, $Si_xC_yN_z$, and CVD deposited material with a low CMP polish rate.

Claim 19. (original) The electrical interconnect structure of claim 1, wherein said first low-k dielectric is an organic dielectric, and said spin-on low k

CMP protective layer is an inorganic material or an inorganic/organic hybrid material.

Claim 20. (original) The electrical interconnect structure of claim 1, wherein said first low k dielectric is porous.

Claim 21. (original) The electrical interconnect structure of claim 1, wherein said first low k dielectric is a stack of dielectric containing an embedded etch stop.

Claim 22. (original) The interconnect structure of claim 1, wherein said first low k dielectric layer has a thickness of from about 600 Å to about 8000 Å.

Claim 23. (original) The electrical interconnect structure of claim 1, wherein said spin-on low k CMP protective layer has a thickness from about 50 Å to about 500 Å.

Claim 24. (original) The interconnect structure of claim 1 wherein said substrate is a semiconductor wafer having an adhesion promoter layer formed thereon.

Claim 25. (original) The electrical interconnect structure of claim 1, further comprising:

a stack of dielectric layers on said substrate, said stack including at least said first low-k dielectric layer and said spin-on low k CMP protective layer.

Claim 26. (original) The electrical interconnect structure of claim 25, further comprising: a plurality of patterned metal conductors formed within said

stack of said first low-k dielectric layer and said spin-on low k CMP protective layer.

Claim 27. (original) The electrical interconnect structure of claim 26, wherein at least one of said patterned metal conductors is an electrical via.

Claim 28. (original) The electrical interconnect structure of claim 27, wherein at least one of said patterned metal conductors is a line connected to said via.

Claim 29. (original) The electrical interconnect structure of claim 25, further comprising:

a single level of patterned metal conductors formed within said stack of dielectric layers on said substrate.

Claim 30. (original) The electrical interconnect structure of claim 29, wherein said patterned metal conductors is a line.

Claim 31. (original) The electrical interconnect structure of claim 29, wherein said patterned metal conductors is a via.

Claims 32-50 (canceled)